In the Claims:

Please cancel claims 1, 4-7, 18-19, and 21-23. The claims are as follows.

1. (Canceled)).

2-3. (Canceled)

4-7. (Canceled)

8-10. (Canceled)

11. (Previously Presented) A method, comprising:

providing a processor;

providing M independent vector register files within the processor; storing a matrix of L data elements in the M vector register files, each data element having B binary bits, said matrix having N rows and M columns, said L=N*M, said N=K*M, each column having K subcolumns, said $N \geq 2$, said $M \geq 2$, said $K \geq 2$, said N=K*M, said $B \geq 1$, each row of said N rows being addressable, each subcolumn of said K subcolumns being addressable, said processor not duplicatively storing said L data elements; and

wherein M multiplexors are coupled to the M vector register files such that each of the M multiplexors has a different value, wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented

by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits,

wherein the method further comprises providing M address registers within the processor, wherein each address register of the M address registers is associated with a corresponding one of the M vector register files, wherein each of the M vector register files includes an array of N registers, wherein each of the N*M registers of the M vector register files stores a data element of the L data elements, wherein each vector register file is independently addressable through its associated address register being adapted to point to one of the N registers of said vector register file,

wherein the data elements of each subcolumn are stored in different vector register files, and wherein the data elements of each row are stored in different vector register files.

12. (Original) The method of claim 11, wherein the data elements of each subcolumn are stored in different relative register locations of the different vector register files, and wherein the data elements of each row are stored in a same relative register location of the different vector register files.

13. (Previously Presented) The method of claim 11, wherein the M multiplexors are adapted to respond to a command to read a row of the matrix by mapping the data elements of the row from the M vector register files to the row of the matrix in accordance with a read-row mapping algorithm; and

wherein the M multiplexors are adapted to respond to a command to read a subcolumn of

the matrix by reading the data elements of the subcolumn from the M vector register files to the subcolumn of the matrix in accordance with a read-subcolumn mapping algorithm.

14. (Previously Presented) The method of claim 11,

wherein the M multiplexors are adapted to respond to a command to write a row of the matrix by mapping the data elements of the row to the M vector register files in accordance with a write-row mapping algorithm; and

wherein the M multiplexors are adapted to respond to a command to write a subcolumn of the matrix by mapping the data elements of the subcolumn to the M vector register files in accordance with a write-subcolumn mapping algorithm.

15. (Canceled)

16. (Previously Presented) The method of claim 11, further comprising addressing a row of the N rows.

17. (Previously Presented) The method of claim 11, further comprising addressing a subcolumn of the K*M subcolumns.

18-19. (Canceled)

20. (Canceled)

21-23. (Canceled)

24. (Canceled)

25. (Canceled)

26-32. (Cancelled)